A Multi-Mode Pixel with Photodiode and Clock-Recharged SPAD Operation for Continuous Recording Applications

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***Abstract*—We present a multi-mode, high-dynamic-range (HDR) photodiode (PD) pixel architecture designed for continuous optical signal recording and high-frame-rate applications. Recent advances in image sensor technology face challenges in achieving a wide dynamic range. Our proposed sensor structure addresses these limitations by enabling operation across different sensitivity regions of the photodiode. By adjusting the pixel bias voltage, the sensor can function in three distinct modes: low-sensitivity & high-sensitivity PD, a narrow avalanche photodiode (APD) region, and a clock-recharged single-photon avalanche diode (SPAD). This design offers flexibility in exposure time per cycle and recharge frequency. Photon detection is read out via a source follower and digitized through an analog-to-digital converter (ADC), allowing for continuous photon arrival timestamping with microsecond to millisecond resolution depending on ADC sampling rate and resolution. The sensor is fabricated using a 3D-stacked $65\,\mathrm{nm}/40\,\mathrm{nm}$ imaging process, achieving approximately a 10× sensitivity increase when varying the bias voltage from $-3\,\mathrm{V}$ to $-17\,\mathrm{V}$. This advancement supports HDR ranging from single-photon sensitivity to illumination levels as high as $500\,\mathrm{\mu W\,cm^{-2}}$.**

I. INTRODUCTION

Image sensor applications span multiple fields, including autonomous edge/IoT devices, outdoor navigation, neural recording, and healthcare technology, such as photoplethysmography (PPG). These diverse applications operate under varying lighting conditions, imposing dynamic range requirements on image sensors. Several approaches have been proposed to address the HDR camera challenge; however, they either require additional in-pixel circuits to modify the lengths of the exposure window [1] or rely on complex algorithms to reconstruct the response of the image light [2].

In this work, we propose a pixel that integrates three operational modes—PD, APD, and SPAD—to achieve a high dynamic range vision sensor, as previously demonstrated in [3]. SPADs operate in Geiger-mode, offering single-photon sensitivity, digital output, and ultra-low readout noise, making them particularly suitable for imaging applications. Recent SPAD-based imaging applications include low-light imaging [4] and fluorescence lifetime imaging (FLIM) [5]. However, these applications primarily utilize only the SPAD mode—the most sensitive region of the pixel. By lowering the bias voltage, the pixel transitions into the PD and APD regions, which exhibit lower sensitivity and are less prone to saturation in high-light conditions, thereby extending the dynamic range.

By simply adjusting the bias voltage, the pixel can seamlessly transition between these operational modes, providing an efficient, hardware-friendly method to extend dynamic range. Additionally, the analog output supports on-chip analog computing, enabling new possibilities for real-time signal processing. Unlike conventional CMOS image sensors, SPAD-based sensors offer faster response times, lower readout noise, and continuous light capture without losses during reset or output transfer. With its enhanced dynamic range and real-time signal acquisition, the proposed pixel is well-suited for continuous signal recording applications such as medical imaging and bio-imaging [6], where uninterrupted, high-fidelity signal acquisition is critical. This capability aligns with our future application goals.

II. ARCHITECTURE

The prototype continuous recording pixel with a kS/s off-chip ADC capturing the pixel output trace over time is illustrated in Figure 1(a). The pixel employs a simple and practical circuit that can easily be implemented in a large pixel 3D-stacked imager format. A PMOS (M_{RST}) serves as either a variable resistor with a gate bias voltage or as a pulsed/clocked recharge switch. The source follower M_{SF} reads out the voltage from the pixel's cathode.

Figure 1(b-c) shows the future application goal of a wide-field imager system capable of streaming image data and parallel optical signal traces (at kS/s), such as for neuro image recording simultaneously to provide low latency and low artifact signals to the processor.

As shown in the expected I/V curve in Figure 2(a), the pixel can operate in three regions by setting the pixel bias for varying light sensitivity: low and high sensitivity PD, a narrow APD region and Geiger-mode SPAD. When the M_{RST} is biased to operate as a resistor, the pixel output decreases as the light intensity—represented by the photocurrent—increases. The sensitivity is controlled by the bias voltage, as illustrated in Figure 2(b). When M_{RST} has a gated bias, the expected V_{out} of low-sensitivity PD mode is shown in Figure 2(d). High-sensitivity PD (Figure 2(e)) operates similarly to a 3T-

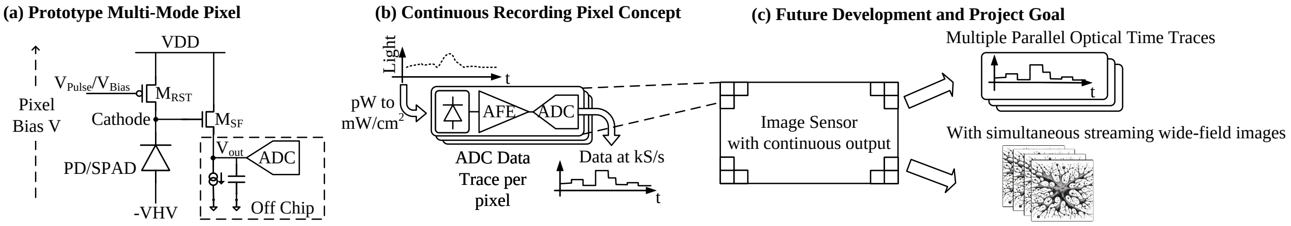

Fig. 1: (a) Multi-mode pixel circuit structure. (b) Pixel concept, incorporating a front-end circuit and ADC for continuous analog data readout. (c) Future development goal: a wide-field imager capable of streaming images while simultaneously outputting parallel optical traces.

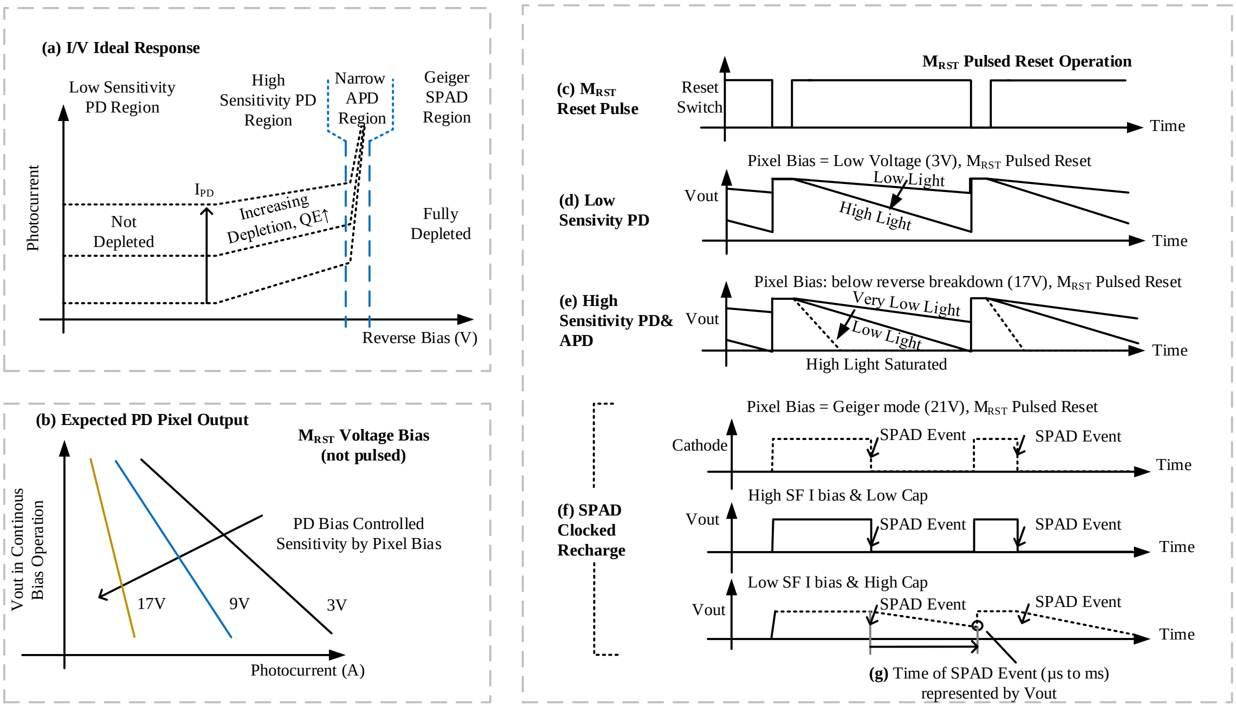

Fig. 2: (a) Ideal I/V response (b) M_{RST} with voltage bias act as a resistor provides a continuous voltage output dependent on light level and VHV bias. (c) Reset switch timing same for all modes of pulsed operation. (d) Photo diode response shown in V_{out} timing diagram. (e) Increased pixel sensitivity with pixel bias near to breakdown. (f) Clocked recharge SPAD operation. (g) The time of photon arrival can be obtained by voltage measurement before the following recharge.

pixel with continuous operation. A timed reset pulse (a short periodic dead time in the recording trace), and the linear photodiode discharge is shown. The scheme's advantage is that the kTC noise present during reset becomes a time-varying offset for each discharge phase (sampled multiple times by the ADC) and can be removed. When the bias voltage exceeds 19V, the pixel transitions to SPAD mode, achieving single photon sensitivity. Figure 2(f) shows the clocked-recharge SPAD, realized with higher frequency reset pulse applied to the M_{RST}. There is flexibility in exposure time per cycle and recharge frequency, addressing saturation issues caused by long cycles and insufficient exposure time in short cycles. In this work, the clocked recharge SPAD operation is read out through the source follower and quantified by ADC. However, in real-world conditions, the source follower may exhibit deviations due to non-ideal current biasing. Under low I_{bias} conditions, V_{out} declines more slowly, potentially impacting the accuracy of the recorded signal.

III. EXPERIMENTAL SETUP AND RESULTS

The implementation utilizes ST Microelectronics 3D-stacked 65 nm/40 nm imaging process without process modification [7]. The pixel pitch is 81.36 µm with 8×8 N+/P SPADs connected in parallel on the top tier wafer, stacked over the pixel transistors on the bottom tier wafer. The experimental setup (Figure 3) includes an off-chip continuously sampling ADC. Two power supplies are used to provide 3.3 V and a negative high voltage for the pixel.

The measurement in Figure 4 matches well with expected I/V curve, demonstrating an approximately ten times increase

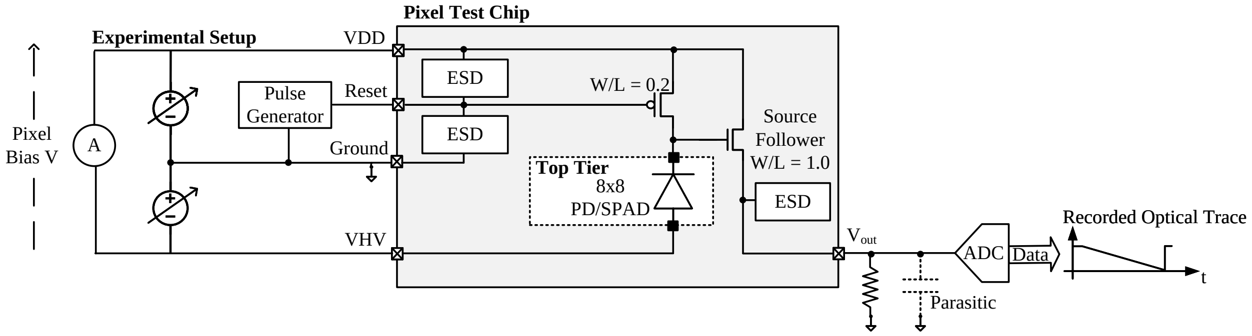

Fig. 3: Experimental setup of the multi-mode pixel test chip. A resistor has been used to bias the source follower, and in addition there is an ESD protection structure with voltage-dependent variable capacitance which together cause non-linearity in the output time traces in Figures 7 to 9.

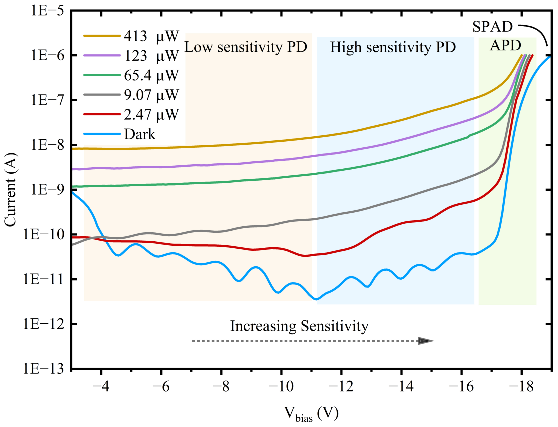

Fig. 4: Pixel I/V measurement at varying light levels and dark scene. Sensitivity increases with rising bias voltage.

in sensitivity between -3V and -17V. As the bias voltage increases, the operating region of the device transitions through distinct modes: from a low-sensitivity PD to a high-sensitivity PD region, then to a very narrow APD region, and finally reaching the SPAD mode when exceeding -19V.

Figure 5 shows responsivity changes according to V_{bias}. In PD regions, responsivity in log-scale increases linearly with bias voltage. In the APD region, responsivity exhibits exponential growth due to the avalanche effect. As the voltage increases further, responsivity is highest in SPAD mode. In this experiment, the current through the device is limited for protection. As a result, when the current becomes significantly large and is above the current limit, responsivity measurement is not captured in the SPAD region.

Figure 6 displays the output when M_{RST} functions as a resistor, with light power versus V_{out} for varied pixel bias. As light intensity increases, V_{out} approaches zero, exhibiting a linear response to illumination. The observed nonlinearity when the device cathode drops below V_{th} may stem from the nonlinear bias current I_{bias} of source follower.

Figure 7 and 8 show the PD region with pulsed reset at two different bias voltages (-3V and -17V) and the different pixel sensitivity is evident.

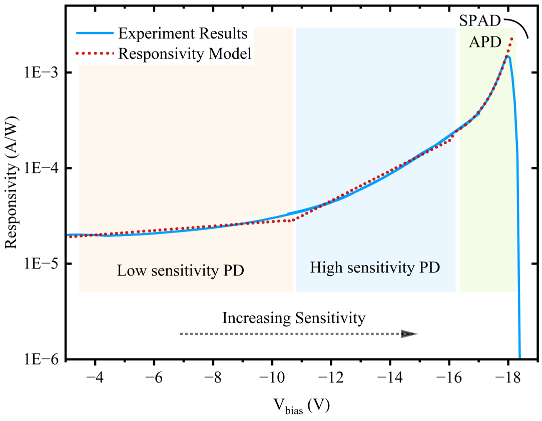

Fig. 5: Pixel responsivity across a range of bias voltages: In the PD region, responsivity increases linearly with bias voltage. In the APD region, it exhibits exponential growth. As the voltage increases further, responsivity reaches its maximum in SPAD mode.

Figure 9 demonstrates the waveform of a SPAD operating under a -20.5V bias with clocked-recharge. The arrival of a photon is observed by the onset of the V_{out} discharge, and a time-to-amplitude reading (µs accuracy) may be made by sampling the voltage at the following reset pulse. The V_{out} fast recharge is from the pixel source follower, while the slow non-linear discharge is through the off-chip resistor.

IV. CONCLUSION

This work introduces a versatile pixel structure that integrates low- and high-sensitivity PD, APD, and clock-recharged SPAD, enabling seamless operation across a wide range of light conditions. By incorporating multiple sensitivity regions within a single pixel, it enhances adaptability to varying illumination environments. Its flexible exposure time and recharge frequency effectively mitigate saturation in long cycles and insufficient exposure in short cycles. Future work will focus on achieving high-sample-rate continuous signal recording in bio-medical applications. This innovative pixel design provides a promising analog front-end solution for next-generation imaging and optical sensing applications.

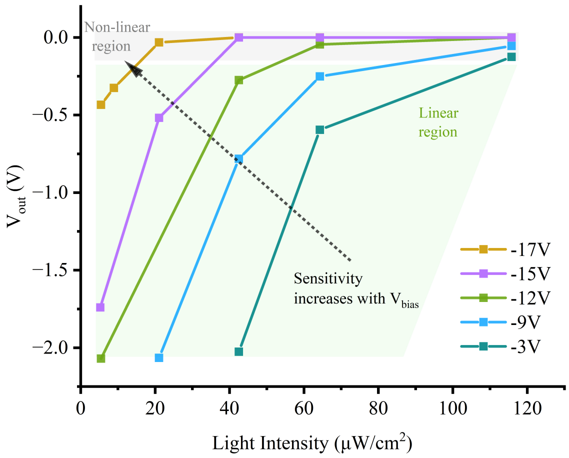

Fig. 6: Measured photo-diode operating voltage with M_{RST} biased and not pulsed. V_{out} drops with increasing light current. The non-linearity may be attributed to the source follower's bias current.

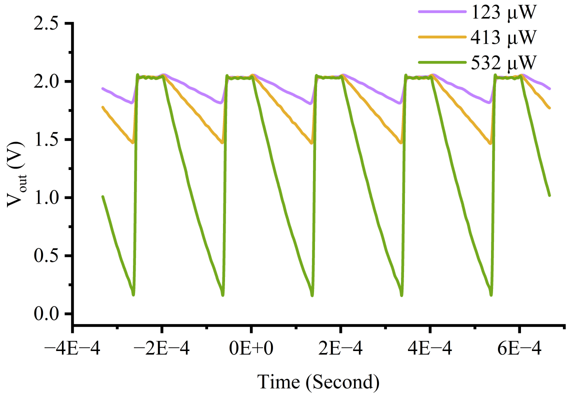

Fig. 7: Measured low sensitivity photo-diode operation with pulsed reset for continuous recording. Pixel bias = -3V.

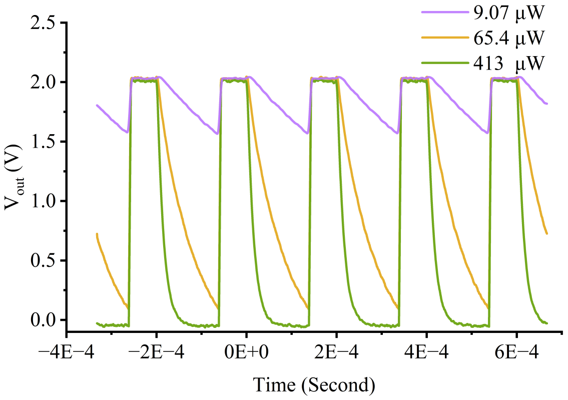

Fig. 8: Measured high sensitivity photo-diode operation with pulsed reset for continuous recording. Pixel bias = -17V. The non-linear discharge is caused by the use of a resistor to bias the source follower and the ESD structure at its output. The bias current is affected by the V_{out} voltage.

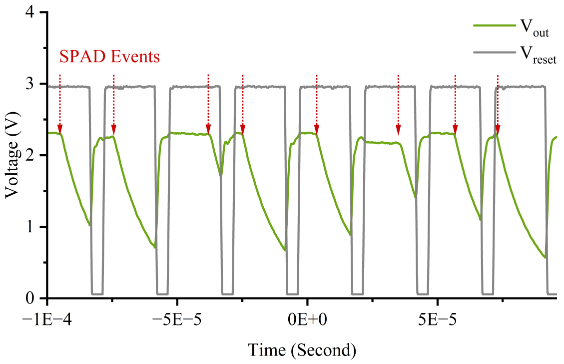

Fig. 9: Measured clocked-recharge SPAD operation in darkness with a pixel bias of -20.5V. The black line represents the reset pulse, while the green line shows the source follower's voltage output.

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